

Design and Implementation of High Precision Synchronization Controller for Gated Imaging

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Abstract

In this paper, we have designed a high-precision synchronization controller for gated imaging. The design scheme is proposed according to the semiconductor laser arrays overall range-gated imaging system composition and working principle. The programming of control logic is illustrated in detail from the main time counter, mode control logic, key control decoder, pulse generator, automatic frequency generator and display control. Finally, a synchronization controller with precision of 80 ns and frequency of 12 khz was developed. The whole system joint debugging test shows that the indicators of the synchronization controller have reached the expected goal, and have met the current technical requirements of gated imaging within 3 km in the atmospheric environment.

Keywords: range-gating, synchronization control, laser imaging, CPLD, step delay

I. Introduction

Since the laser was introduced into the imaging system in the 1970s, laser active imaging has become a research hotspot in many countries for its advantages of long imaging distance and clearer imaging.^[1-4] However, in the process of laser imaging, as the imaging distance becomes longer, the image quality is affected more seriously by the backscattered light produced by atmospheric molecules and suspended particles, which seriously restricts the application of the imaging system.^[5] Range gated imaging technology is based on controlling the relative delay between gating and laser pulse, which can realize the target imaging at a specific distance. This technique enables the imaging system to capture only the reflected (scattered) light from the target area.^[6-9] Because the atmospheric backscattered light and other background stray light are filtered out in the process of propagation, range gated imaging has the advantages of clear imaging, high contrast, strong anti-interference ability and no influence of ambient light. This method is widely used in remote sensing image analysis, military reconnaissance, robot navigation and industrial exploration.^[10-14]

There are many organizations studying range gated laser imaging technology at home and abroad. The Danish defense research agency uses the delay stepping method to illuminate the same target in different delay time to obtain the contour and distance information of the image. However, the laser energy of the device is low, and it cannot image remotely.^[1] The laser range gated imaging products of Canadian company can realize long-distance monitoring. The recognition distance for face is 8 km, and the recognition distance for car is 10 km.^[3] The imaging system produced by American company can obtain the target image at 28 km, and it is small in size and easy to carry. At present, it has been widely used.^[2] Among the existing products and published research results, the synchronization control index for range gated laser imaging system varies with the operating distance of the system. The gate width and step accuracy vary from several nanoseconds to hundreds of nanoseconds, and the technical routes are also different.^[15-17] In the gated imaging system, in order to achieve the goal of range gating, it is necessary to synchronize the exposure time of the imaging system with the luminous time of the laser light source accurately. Therefore, the development of a time synchronization controller with precise time control

function to accurately control the action time of the imaging system and the laser light source system has become a key technology to realize the range gated laser imaging system.^[18-21] In this paper, the overall index of the system has special requirements for the operating range and range resolution. Considering the mass production cost, we design and implement a synchronous control device to meet the index requirements.

II. Overall Design of Range Gated Laser Imaging System and Requirements for Synchronization Controller

The range gated laser imaging system designed in this paper is mainly composed of laser transmitting, receiving imaging, synchronous control and signal image processing. Its composition is shown in Figure 1. The laser emission system is composed of emission optical path, laser and laser controller, which can complete the functions of laser beam emission and shaping; The receiving imaging system consists of ICCD, ICCD controller and video synthesizer, which is used to receive and amplify laser echo, detect target image and synthesize standard video signal for display; The synchronous control part completes the synchronous signal setting, generation, delay time calculation, fine-tuning and other functions; The signal image processing part completes the functions of real-time image processing, storage and display.

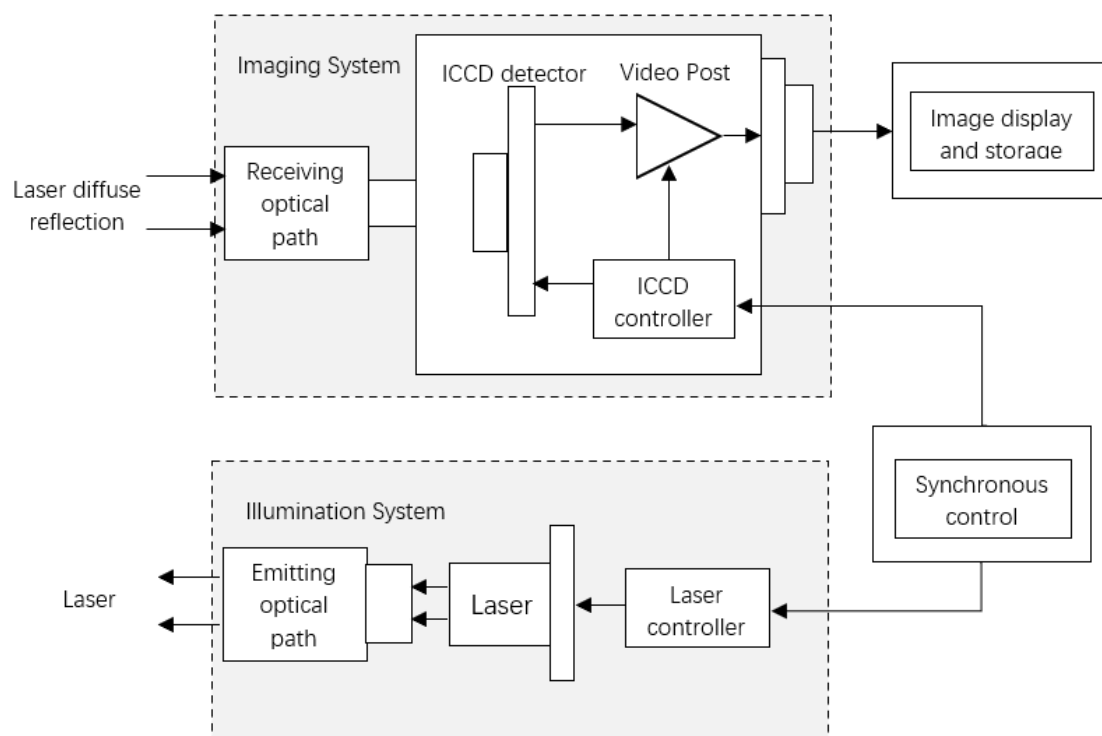


Fig.1: Block diagram of range gated laser imaging system

Its working principle is: according to the target distance obtained by the ranging module, the delay time needed for range gating is calculated, and the laser pulse width and ICCD exposure time are set according to the required reconnaissance depth of field. The central synchronous control module sends the set trigger pulse to the laser controller, i.e. the laser driving power supply, modulates the laser power supply to make it send out a certain frequency laser pulse, and sends the same period exposure trigger signal after precise delay to the ICCD to realize the distance gating of the shutter to the echo signal. The imaging system accumulates the received target echo according to a certain repetition rate, synthesizes the echo signal into an image signal with a certain frame rate, and outputs it to the image display and storage module. For real-time imaging and image post-processing.

According to the overall index of the system, the gating imaging system has the following requirements for the synchronization control part: (1) The maximum delay time is not less than 20 μ s; (2) The maximum pulse width is not less than 20 μ s; (3) The minimum pulse width is not more than 100ns; (4) Self trigger and external trigger

function.

III. Overall Design of Synchronous Controlle

3.1 Chip Selection

We use the control circuit chip of CPLD time synchronization controller, which only needs one chip to complete the control of the system. In this way, we can make full use of the circuit board space and make the system miniaturized. At the same time, the fixed delay of CPLD will reduce the risk of timing competition and provide more stable control timing.

CPLD devices need enough resources to provide the control signals needed by the system, and at the same time, they need to have surplus resources to expand the system. According to the functional requirements of the system, the control chip needs at least mode, set and up buttons; It has control signal interfaces such as trig, out-width and out-delay; It also needs to display the current system status, including pulse width setting, delay time setting, frequency setting and working mode; In addition, the system also displays the delay time, pulse width and system frequency, which can be realized by 8-segment digital tube. Therefore, the control chip needs at least $4 + 3 + 16 = 23$ I / O pins. In addition, in order to ensure the reliability and scalability of the system, the internal connection resources and macro unit resources of the control chip should be enough, that is, the number of macro units should be more than twice the number of I / O pins, that is, 46. These are the resources that CPLD should provide at least. In order to achieve high time control accuracy, the system's working clock frequency is up to 50 MHz, providing 20ns time accuracy, and its working voltage is 4 V. Therefore, the control chip should be able to work under 50MHz clock signal, which meets the low voltage standard.

According to the general requirements, a CPLD device of Xilinx company is selected as the control chip. The working voltage of the chip is 4 V, it contains 144 macro cells, 81 available I / O pins, 10ns pin to pin fixed delay, the highest clock frequency is 178mhz, its I / O pins can accept 5 V, 4 V, 2.5 V logic signal, and output 4 V level logic signal, which meets the system requirements.

3.2 Overall Structure of the System

The system time synchronization controller has two basic functions: active pulse output and time delay pulse output. The frequency, pulse width and delay time of the generated pulse can be controlled to control the correct action time of the laser and imaging system. It is mainly composed of core CPLD control chip, nixie tube display unit, key operation unit and output interface. All the signal and control operations are completed by the CPLD control chip. Nixie tube display unit is used to display pulse width, frequency, delay time and other information. The key unit is used for human-computer interaction to set the time parameters of the system. Its structure block diagram is shown in Figure 2.

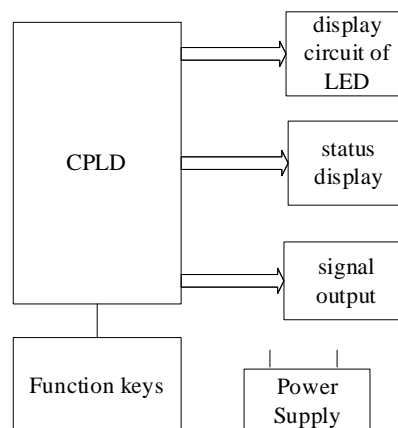


Fig.2: System structure block diagram

According to the overall requirements of the system, CPLD logic control program should have the following functions: 1. Self triggering and external triggering. That is to say, the controller automatically generates the pulse signal of corresponding frequency when it is triggered, and its width and time delay are the same as the set value; When the external trigger signal is triggered, the controller generates a group of pulse signals that meet the set value when the rising edge of the external trigger signal comes. 2. Laser control pulse width setting function. That is, the width of the output laser control pulse can be set, and the length of the laser light emitting time can be controlled. 3. The imaging system controls the pulse delay time setting. It is used to set the delayed opening time of the imaging system to achieve the effect of range gating. 4. System working frequency setting. It is used to set the system frequency when the repetition frequency works, which can improve the detection range of the system. 5. Status display function. It can display the current pulse width, delay time, setting value of working frequency and current working state.

According to the function analysis of CPLD, the program design function block diagram is designed, and the data flow analysis, control signal analysis and program flow design of each main part are carried out to realize the above functions. The internal logic block diagram is shown in Figure 3.

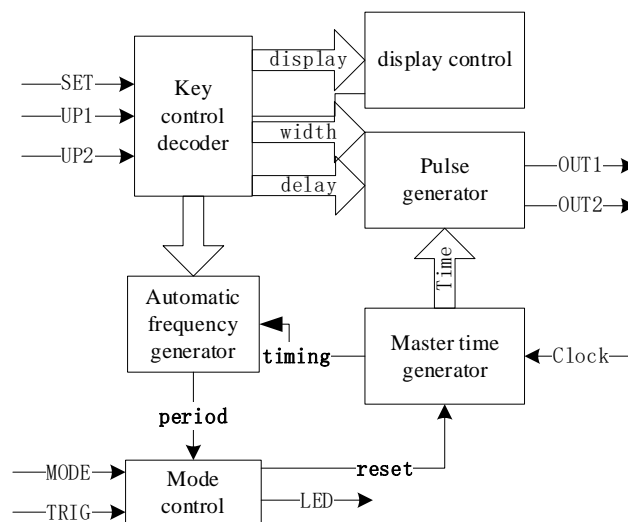


Fig.3: Internal logic block diagram of CPLD

The main time counter is used to generate the internal standard time to control the pulse generator to generate the corresponding pulse output. The mode controller is used for external trigger and self-trigger control. The corresponding working mode is set according to the key and displayed by LED. The key control decoder can decode the key input signal and store the set value of the key to realize the correct control of the key input signal. The frequency controller is used to configure the working frequency of the system and generate the control pulse of the corresponding frequency according to the value set by the key. Pulse generator is the core program of the system, which generates the corresponding output pulse according to the time counter and key setting value, and controls the external laser and imaging system to work correctly. The display control unit is used to control the normal operation of the system display unit, which includes the control of a group of 8-segment digital display tubes and 4 LED status indicators.

IV. Programming of Control Logic

4.1 Master Time Counter

The master time counter is a standard time generator. Zero represents the leading edge time of laser emission pulse,

and its numerical value represents the time length of the current system after laser emission, and also represents the laser transmission distance. The counter is a one-way self-increasing counter. When the value is greater than a certain value, it means that the laser has been transmitted beyond the detectable distance of the system, and the counting stops. When a trigger pulse needs to be given to the laser, the counting starts from zero, and each system clock counts once. When the main clock of 50 MHz is used, it means that the time has passed 20 ns. It consists of clear logic, counter logic and output. When the clearing logic determines the system zero, it is a synchronous clearing pulse; The counter logic is a 13 bit binary counter with the maximum value of 163 us, which can generate a time control signal with a step size of 20 ns; The output is a 13 bit binary parallel data tnumq (12:0), which internally represents the current system time and provides standard time data for pulse generator and other logic. Its structure is shown in Figure 4.



Fig.4: Structure of main time counter

4.2 Mode Control Logic

Mode control logic is a program code responsible for mode selection in the time synchronization controller. Its function is to respond to the external mode setting key and configure the system working mode according to the current state. The system has two working modes: automatic trigger mode and external trigger mode. When the mode selection key is pressed, the system switches between the two modes. For example, when the current mode is automatic trigger mode, pressing the mode selection key will set the system to external trigger mode. The working state of the system is displayed by the mode indicator LED. When the mode indicator LED is on, it indicates that the system is in the external trigger mode, otherwise it is in the automatic trigger mode.

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4.3 Key Control Decoder

The key control decoder is used to analyze the control commands of set, up1 and up2. According to the commands, the pulse width, delay time and working frequency are set and stored in CPLD. At the same time, the setting information is sent to the pulse generator unit. In addition, the data to be displayed is sent to the display control unit. When the set key is pressed, cycle the settings of pulse width, delay time and working frequency. Up1 increases the high value to be set and up2 increases the low value to be set. The settings of the three states are internally represented by 13 bit binary values, corresponding to 39 internal registers. The key control decoder structure is shown in Figure 5.

In the actual debugging process, it often occurs that the value of a key changes many times. This is because the key switch inevitably produces some small jitters in the process of manual pressing. These jitters are often microsecond sequence pulses, and the internal digital circuit has no ability to resist microsecond interference. Therefore, a key

filter is specially designed in the control decoder, It is used to filter the clutter generated by key jitter, so as to provide normal key signal.

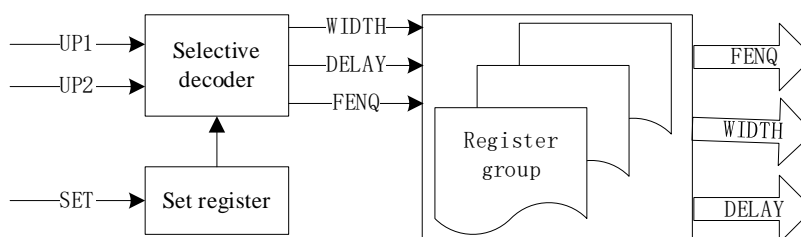


Fig.5: Key control decoder structure

4.4 Pulse Generator

Pulse generator is the core of the program, which can produce a group of pulse signals with specific requirements. In the self triggering mode, two pulse signals with precise delay are output to control the external laser and imaging system; In the external trigger mode, after the received laser pulse signal is accurately delayed, a delay pulse is output to control the shutter exposure time of the imaging system.

In the self triggering mode, the standard time data is obtained by the time generator, and then the pulse width and delay time data set by the operator are obtained by the key control decoder. The correct pulse output time and stop time are obtained by calculation.

The first pulse signal (out1) is used to modulate the power supply of the semiconductor laser. The time of laser pulse emission is triggered by the rising edge of out1, and the pulse width is equivalent to that of out1 (there is a certain nanosecond circuit fixed delay. The imaging system in this paper is designed for remote gated imaging, and the delay time is usually in the microsecond level, which can be ignored. If it is used in close range gated imaging, the delay precision of synchronization controller is set to 10 nanoseconds, and most of the influence of fixed delay on gated imaging is offset by adjusting the delay time. Based on the rising edge of out1, the second pulse signal (delayed pulse signal out2) is output after accurate delay according to the set delay time to control the exposure time of the imaging system (the exposure time is set by the imaging system).

The timer 1 obtains the pulse width data from the key control decoder, and calculates the trigger (outtrig) and stop (outstop) time of pulse 1 (out1) with the standard time data. Under the control of outtrig and outstop signals, the trigger register generates the pulse signal (out1) with the set width at the corresponding time to realize the setting and adjustment of the output pulse width.

The processing of delay pulse is similar to this. Timer 2 obtains pulse delay data and standard time data, calculates the trigger (out2tig) and stop (out2stop) time of delay output pulse (out2), and generates delay trigger pulse at corresponding time through trigger register with fixed width. This is because the exposure of imaging system is triggered by rising edge, The exposure time is set by the camera control program. Therefore, the delay pulse can achieve the desired effect of the system only when the leading edge time is accurate.

See Figure 6 for the working state of the specific implementation. In the oscilloscope, channel 1 (yellow) is the modulation pulse of laser power supply (out1), and channel 2 (blue) is the delayed trigger pulse of imaging system (out2).

When the external trigger mode works, it does not need to generate the first pulse signal (out1), but only needs to take the received laser pulse signal as the reference, delay according to the set delay time data obtained from the key control decoder, and output the delayed pulse signal (out2).

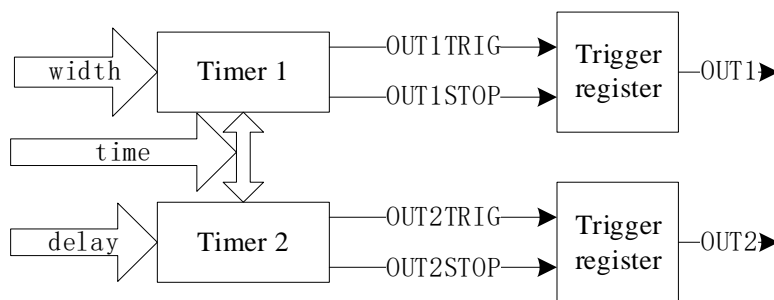


Fig.6: Structure diagram of pulse generator

4.5 Automatic Frequency Generator and Display Control

The automatic frequency generator obtains the standard time data and frequency setting data, and calculates the time. When the total time and frequency setting cycle are the same, a time end pulse signal is generated. This signal is sent to the mode control unit as a cycle signal, which decides whether to clear the total time counter. When the periodic signal is used to clear the time generator, the system will run at a certain frequency and generate the corresponding pulse output.

System display control is an important part of human-computer interaction, it can display the current system set frequency, pulse width, delay time value. The display unit is mainly composed of a group of two 8-segment nixie tubes and four LEDs. Its control is completed through 13 data lines, 10 for 8-segment nixie tubes and 4 for LEDs. Because the two nixie tubes share the same data line, it is necessary to display the two nixie tubes with time-sharing power supply. In the design, two nixie tubes are selected by the chip selection signal, and different nixie tubes are selected at different times, and the corresponding data is sent to the data line, so that the two nixie tubes display different values. Because of the visual persistence effect, when the refresh frequency is higher than 60 Hz, there is no obvious flicker phenomenon in the two nixie tubes. In the design, the frequency of 100 Hz is used to refresh the data, and a better display.

The binary 8-bit data of pulse width, delay and frequency obtained by display control can not be directly used for numerical display of nixie tube, so decoding is needed to display the numerical value correctly. In the design, the internal logic adopts the design of hexadecimal decoder, which shows the hexadecimal effect. Therefore, in the specific numerical calculation, a conversion is needed to get the actual value of delay or pulse width.

V. Main Target and Conclusion

The completed synchronization control system is shown in Figure 7A, and the delay effect is shown in Figure 7B.

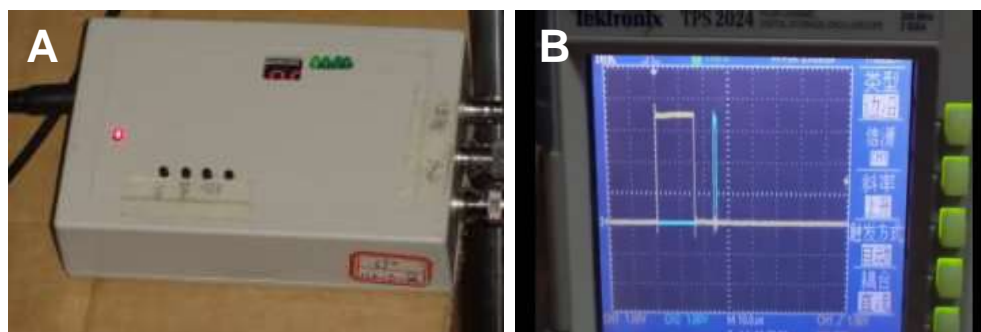


Fig.7: (A) High precision synchronization controller based on CPLD; (B) Precise delay effect of pulse signal.

Figure 7A shows the oscilloscope display picture of the two pulse signals during the whole system joint debugging, in which the signal channel 1 (yellow) is the laser power supply modulation pulse (out1), and the channel 2 (blue)

is the delayed imaging system trigger pulse (out2). The width of out1 is 15 μ s, because the power of the semiconductor laser array we used at that time is larger, about 1500 W, and the laser power supply has limited driving capacity, which can not drive the pulse width less than 15 μ s. Therefore, the gating can only be realized by precisely controlling the exposure time of the shutter of the imaging system, that is, only receiving the laser energy at the tail of the laser pulse for a short period of time.

Our CPLD control chip can support up to 10 ns precision. Considering the complexity of the program and the stability of the system, the highest performance of the same control system is as follows: Pulse width and delay time: step length 20 ns, 256 steps; Pulse width adjustment range: 20 ns \sim 5.1 μ s; Delay time adjustment range: 20 ns \sim 5.1 μ s.

Among them, the step size can be increased by 20 ns by modifying the program parameter setting, and the corresponding adjustment range will also be increased.

According to the overall requirements of the system, the final program indicators are set as follows: Pulse width and delay time: 80 ns step, 256 steps; Pulse width adjustment range: 80 ns \sim 20.5 μ s; Delay time adjustment range: 80 ns \sim 20.5 μ s; Frequency regulation range: 1.6 hz \sim 12 khz.

The operation results show that the width, frequency and delay of the synchronous controller meet the overall requirements. The joint commissioning test of the whole system shows that the indicators of the synchronous controller have reached the expected goal, and have met the current technical requirements of gated imaging within 5 km in the atmospheric environment. However, the application of range gated laser imaging technology in near-range underwater imaging and non-visual imaging is in the ascendant, which requires shorter pulse width, more accurate delay control and multi-channel delay output. Therefore, there is still a further research value in picosecond control accuracy and multi-channel parallel output.

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